# Wideband recording

Saturn currently has no wideband recording mode. Thetis expects a recording to be made periodically of a block od continuous ADC samples, and the data be transferred in special packets. The parameters are specified in the general packet. Recording duration and period can be specified. Data could be recorded from either ADC.

## Potential Saturn Implementation

Implement an IP that records data into a FIFO. Every time a new record starts, clear the FIFO in case of errors. The IP counts samples, and counts a time period before the next recording. Pi software sets up the IP, reads the FIFO when occupied and transfers data back to Thetis.

For efficiency: IP sets a bit when recording complete. The full data set can then be read on one operation. Software re-enables the IP to record the next block; IP records when timeout complete and the enable is set.

For optimum FPGA utilisation if two ADCs to be recorded: space the out 50% in time, so that one FIFO can be used for both. That will work with long periods between recordings, but not short ones (could be set down to 1ms).

## Thetis Parameters

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Location** | **Meaning** | **Default setting** |
| Wideband ADC0 port (15:0) | General packet bytes 21,22 | Base outgoing port number | 1027 |
| Wideband enable[7:0] | Byte 23 | Enable for each ADC (bit 0=ADC1) | 0 (Thetis only enables ADC0) |
| Wideband samples per packet [15:0] | Bytes 24, 25 | Samples to be transferred in 1 packet | 512 |
| Wideband sample size | Byte 26 | Sample resolution  (0 means 16 bits) | 16 bits |
| Wideband update rate | Byte 27 | Period between recordings in ms | 20ms (Thetis seems to set 70ms, or 15 updates / s) |
| Wideband packets per frame | Byte 28 | Number of complete packets per recording | 32 (ie 16K samples) (Thetis gives options for 8 or 32) |

## Changes Needed

Create New IP

IP mapped into Axi-4 Lite memory map

FIFO attached to the IP that allows it to be read onto AXI-4

That IP mapped into AXI-4 address space

# Wideband IP

## Function

1. When enabled by software
   1. start a timeout count for next recording
   2. record a block of samples from 1st enabled ADC of programmed duration.
   3. Set a flag to tell software
2. When data has been read out
   1. If another ADC is enabled, repeat from step b
3. If no more ADCs enabled, wait for next timeout && enabled.

## Interfaces

AXI4-Lite bus interface

AXI4-Lite registers

2x16 bit ADC inputs (continuous not stream)

Output stream to FIFO (64 bits)

FIFO reset output

Potentially interrupt output